4. RISK FACTORS

Before investing in our Shares, you should pay particular attention to the fact that we, and to a large extent of our activities, are subject to the legal, regulatory and business environment in Malaysia. Our business is subject to a number of factors, many of which are outside our control. Before making an investment decision, you should carefully consider, along with other matters in this Prospectus, the risk and investment considerations set out below (which may not be exhaustive) and may have a significant impact on the future performance of our business. Additional risks, whether known or unknown, may in the future have a material adverse effect on us or our Shares.

4.1 RISKS RELATING TO OUR SHARES

4.1.1 Delay in or Failure of Our Listings

We foresee that our listing exercise may be delayed or aborted if the following events occur:

(a) the Underwriter fails to honour its obligations under the Underwriting Agreement in the event of under-subscription; or

(b) the placees fail to honour their obligations to subscribe for the portion of Issue Shares to be placed out to them under this Public Issue despite having given irrevocable undertakings to acquire the Shares allocated to them; or

(c) we are unable to meet the public spread requirement as determined by Bursa Securities including a minimum of 1,000 public shareholders holding not less than 100 Shares each at the point of Listing; or

(d) the approvals of Bursa Securities, SC or any other relevant authorities for the Listing are revoked, withdrawn or cancelled.

Although our Directors will endeavour to ensure the timeliness and success of our Public Issue and Listing, no assurance can be given that the abovementioned events will not occur and cause a delay in or abortion of our Listing.

4.1.2 No Prior Market For Our Shares

At present, there is no public market and prior trading of our Shares. There can be no assurance that the listing of our Shares will result in the development of an active and liquid public trading market for our Shares. The market price, liquidity and trading volume of our Shares may be volatile. As a result, there is no assurance that trading liquidity will develop for our Shares, and that holders of our Shares will be able to sell their Shares and/or at the prices at which the holders would be willing to sell their Shares. There is also no assurance that you will be able to sell your Shares at prices equal to or greater than the price paid for our Shares under this Public Issue.

The Retail Price of RM0.40 per Issue Share was determined after taking into consideration several factors including, amongst others, our financial condition and future prospects of our business and industry. As such, the price at which our Shares will be traded may differ significantly when traded on the MESDAQ Market of Bursa Securities.

4.1.3 Delay in Settlement and Trading

After we have allotted our Shares to your CDS Account with Bursa Depository, which would occur at least 2 clear market days before the anticipated date for admission, it may not be possible for you to immediately recover monies paid in respect of the Issue Shares from us in the event that our admission and commencement of trading on the MESDAQ Market of Bursa Securities do not occur. In order for us to return the monies to you in respect of the Issue Shares following their allocation in Bursa Depository, a reduction of our Company's capital would be necessary. This would require a special resolution of our Company and the confirmation of the High Court of Malaya. There can be no assurance that monies can be recovered within a short period of time. However, interest is payable on monies not repaid within 14 days in accordance with Section 243(2) of the CMSA.

4.2 RISKS RELATING TO OUR OPERATIONS

4.2.1 Design Failure

We have been able to deliver our obligations in accordance with the terms of the contract with our customers and ensure that our IC design services meet our customers' requirements. As our Group provides ASIC/SoC design services and IP development specific to customers, we may be subject to risk that our ASIC/SoC design will not satisfactorily perform the function for which they are designed and will not be able to meet performance objectives. This may potentially disrupt the customers' operations and production. As such, there is no assurance that a design liability suit or action will not be taken against us for design failure. In addition, we also cannot assure that unanticipated technical or other problems will not occur which may potentially result in a material delay in the design development.

In the event that we are liable for any special, incidental, consequential or indirect damages resulting from its performance or failure to perform, whether based on contract or negligence, this may have adverse effect on our reputation and may result in a loss of business. Such negative exposure will affect our reputation and financial position. In an industry where branding and reliability are crucial, our market share may stand to be adversely affected should such negative publicity arises.

As part of our design liability risk management, our service agreements with our customers do not contain warranties for our design and have provisions designed to limit our exposure to consequential damages. To date, there has been no incidence of lawsuits in respect of design failure. In addition, the risk of design failure is minimised as customers will conduct its own testing and quality acceptance test before accepting the final design and any design failure detected during such testing will be rectified by us prior to delivery. Continuous quality checking will be given more emphasis to avoid any unwanted negative publicity.

4.2.2 Technology Know-How

Our Directors believe that our success depends on our IPs, unique in-house design methodology and proprietary know-how. As such, we need to protect our concepts, idea, design and documentation relating to our proprietary technology from being used by others. However, we cannot assure that other parties will not independently obtain access to our trade secrets and know-how or independently develop designs or technologies similar to ours.

To mitigate the above risks, we do not provide our source codes, which consist of confidential information to our foundries to protect our proprietary know-how. Furthermore, our employees are bound by their respective confidentiality terms as set out in a separate non-disclosure agreement entered into with our Group. We also maintain a comprehensive log sheet to document our design and updates. If any dispute or claim arises over our IC design, we believe that we would be able to prove in court our proprietary rights over our design.

4.2.3 Outsourced Facilities

For the audited 9-month FPE 2007, 99.4% of our direct cost is derived from the outsourcing of development, design and licensing of certain IPs to Key ASIC Inc and 0.6% of our direct cost is derived from outsourcing of wafer fabrication services to Silterra. These outsourcing were entered into on an arms-length basis to develop and design one-off core IPs required in view that we were only a start-up company. Currently, the test and packaging process of our manufactured chips are also outsourced to our strategic partner, ASAT Holdings Limited. We cannot assure that these facilities are available at all times to match our order requirements and we have no control over their timing and cost structure. Failure by our outsourcing partners to deliver may result in a prolonged lag time between our customers' orders and our delivery time and may also interrupt our business operations.

Outsourcing has became a key trend in our industry which saw an increasing number of design houses outsourcing part or all stages of their design process to independent third parties. This is due to the high capital and labour cost involved and increasing competition which drive companies to reduce costs and shorten time-to-market. Also, our industry entails high expertise to operate and the lack of competitive local IC design support as well as lack of IC design talent both in quantity and experience, has prompted us to outsource our design facilities to overseas expertise which include foundries, and test and packaging houses, all of which are crucial to our operations. In view of this industry norm, it is also part of our business strategy to adopt the outsourcing model as and when required.

Going forward, our Directors are of the opinion that the outsourcing of IP development and design is expected to decline as the basic IPs required for design engagement have been substantially developed in the FYE 2006 and most of these IPs can be re-used for many years. Our cost of sales for the FYE 2006 is RM44 million, while the cost of sales for the 9-month FPE 2007 has declined to about RM14.5 million. Nevertheless, we may continue to outsource certain IP development and design to third parties as and when the need arises and ensure that the arrangements are in the best interests of our Group. Meanwhile, we will continuously recruit experienced technical personnel. We have also taken continuous efforts to strengthen and enhance our relationships with our existing outsourcing partners and also build new relationships. This would provide us with a wider range of outsourced facilities and hence, ensure that our operations continue to run smoothly.

4.2.4 Infringement of Intellectual Properties by Third Parties

A substantial part of our Group's revenue is derived from licensing of our IPs to our customers. At present, our Company owns intellectual property rights in the IPs which protection is accorded by copyright laws and the common law, including the Copyright Act 1987. However, the software may not be accorded similar copyright protection laws elsewhere. Despite copyright laws in Malaysia and other countries in which our Group may operate, such laws may not be adequate or effectively enforced against third parties who violate our Company's copyright by copying or pirating our IPs. Our Company may have to incur unexpected and additional expenses for enforcing its intellectual property rights should such infringement arise in future. This may have an adverse effect on our Group's future financial performance. This risk is however mitigated through constant enhancements of our proprietary software, rendering it difficult for third parties to copy or pirate our IPs.

4.2.5 Inventory Risk

Historically, we have taken a prudent approach to refer some of our end customers to Silterra as we do not have the financial capability to purchase and store wafer for the production of chips after the initial design and development stage. However, since the incorporation of KASSB, we are increasing our direct sales of completed chips and wafer to the end-customers to earn a higher margin and to strengthen our relationships with the end-customers. As such, we might have to bear a higher inventory costs for the completed chips and wafer. In view of the constant change in consumer preferences and demand for consumer electronics products, there is no assurance that our customers will continue their purchases of the completed chips and wafer. As a result, there is a possible risk of slow-moving inventory and higher inventory cost to be borne by us.

Nevertheless, we will strive to balance between sales growth and maintaining a prudent inventory management policy as well as continuously innovating and upgrading our existing products and services to be more competitive and more marketable for the consumer electronics products.

4.2.6 Dependence on Key Personnel

Our continued success depends to a certain extent upon the abilities and continued efforts of our existing Directors, key management and technical personnel. The loss of any member of our Directors or key management or technical personnel could negatively affect our Group's continued ability to manage our operations effectively and competitively.

Our design capabilities depend substantially on the number of skilled, professional and knowledge workers with a high level of competence and commitment. Software engineers, system architects, chip design engineers and developers are highly required in the semiconductor industry. If we are unable to retain our skilled workers, staff replacement costs as well as associated opportunity costs may be considerable.

Our Directors recognise the importance of our Group's ability to attract and retain its key personnel and retain a sufficient number of highly skilled employees. We have in place a human resource strategy, which includes suitable compensation packages and human resource training and development programmes for all supporting employees in all key functions of our Group's operation. We have also made continuous efforts to strategically develop a dynamic and strong management team and groom our personnel in assisting senior key personnel to operate and manage our activities. However, there can be no assurance that the above measures will be successful in retaining key personnel or ensuring a smooth transition should changes occur.

4.2.7 Dependence on Key Customer

Our Group is, to a certain extent, dependent on Silterra due to the significant level of sales made to Silterra. Silterra is in the business of semiconductor manufacturing and operates a wafer fabrication foundry in Malaysia. Silterra recorded a contribution to an aggregate of 84% of our Group's total revenue in the past 9-month FPE 2007, of which 76% revenue from licensing and porting of IP designed specifically for Silterra's semiconductor manufacturing process technology and 8% revenue from commission earned for introducing about half of the end customers to Silterra. In the event that Silterra terminates the existing contract with our Group, we may face risk in the transition from Silterra to a new foundry which may take about 3-6 months and also bear the high switching cost.

Our Directors are of the opinion that in our industry, it is a norm for pure IC design houses to form strategic partnership with independent foundries and subcontract its manufacturing work to pure foundry players. At the same time, it is equally important that our chips are designed specifically into the foundry process technology so that foundries also get wafer manufacturing business. This can be seen as an inter-dependent relationship between the design house and the foundry. Such an outsourcing model allows design houses to concentrate on its R&D resources on the end market without committing capital investments to the escalating cost of maintaining a state-of-the-art fabrication facility. The success of such a business model can be seen in Faraday Technology Corporation, a design service company listed in Taipei Stock Exchange, collaborating with United Microelectronics Corporation, a world leading semiconductor foundry in Taiwan, as well as Global Unichip Corporation, the second largest ASIC design service company, collaborating with its major shareholder, TSMC, a leading foundry, both located in Taiwan.

Emulating these successful business models, we have signed a Foundry Service Sales Representative Agreement with Silterra, whereby we are appointed as marketing representative for Silterra in certain countries, and we will be paid a commission for acquiring the sale of silicon wafers fabricated by Silterra. We have also entered into IP Porting Services Agreement and CPU Agreement with Silterra, whereby we shall provide design services and license of IP to Silterra whilst Silterra shall undertake to manufacture the chips designed by our Group containing the ported IP using only manufacturing process specified in such agreements. Such agreements will not prevent customers from placing orders directly to us. We will also establish new business relationships with other foundries such as Chartered Semiconductor Manufacturing Pte Ltd in Singapore and Semiconductor Manufacturing International Corporation in China as part of our measures to manage our dependency on Silterra.

4.2.8 Changes in MSC Status

We were awarded the MSC status on 14 April 2006 by MDeC. Presently, all MSC status companies are granted financial and non-financial incentives. The MSC status granted to us is subject to continuous fulfilment of certain criteria.

MDeC, being the body responsible for monitoring all MSC designated companies, has the right to withdraw the MSC status of any company at any given time. Given the criteria to be complied, there can be no assurance that we will continue to retain our individual MSC status or that our Company will continue to enjoy or not experience any delays in enjoying the MSC incentives outlined, all of which may materially affect our Group's business, operating results and financial condition. Furthermore, there can be no assurance that the MSC incentives will not be changed or modified in any way in the future.

In addition, in the event that the MSC status is withdrawn by MDeC, we would have to comply with the 30% Bumiputera equity requirement and as such, there may be a potential dilution of shareholdings should an offer for sale or private placement exercise are implemented.

4.2.9 Limited Operating History

We were incorporated on 22 August 2005 while our subsidiary, KASSB, was incorporated on 7 June 2007. Our Group's limited operating history makes it difficult to evaluate the risks and uncertainties, particularly those encountered by companies in the early stages of development in the new and rapid evolving semiconductor industry. However, our Group has proven its capability to generate net profits of RM5.64 million for the audited FYE 2006 and RM12.84 million for the 9-month FPE 2007. In addition, our Group's key management and key technical personnel comprise persons who have been involved in the semiconductor industry for an average of 15 years each. Our Directors believe that the risk of our limited operating history is mitigated by the experience, knowledge and business expertise of our key management and key technical personnel.

4.2.10 Delay in R&D

Our Group is involved in a rapidly changing industry and our success is largely dependent on speed and ability to meet the requirements and expectations of the market. We face the risk of not being able to meet targeted launch dates due to a variety of reasons such as changes to design specifications, human resource constraints, new technology announcement and evolving customers' needs.

Our Group has set up its in-house R&D team to carry out research and development in our design activities. Our Group's R&D team is able to assist and support the implementation of our Group's business plan to meet the demands of our Group's customers. However, completion and successful implementation of R&D may require a long lead-time. Although our Group seeks to mitigate this risk by effectively allocating its resources and focusing on servicing customers and prospects with better return (in order not to exhaust our Group's resources or sacrifice quality of our design development), there can be no assurance that there will not be any delays in the completion of its R&D efforts and that any delays in its R&D efforts will not have any material adverse effect on our Group's business and financial performance.

4.2.11 Significant Influence of the Controlling Shareholder Over Our Business and Policies

Eg Kah Yee will, directly and indirectly, hold 51.31% of our Shares upon completion of the Public Issue. Through his equity interest in Key ASIC, he will be able to influence the outcome of certain matters requiring our shareholders' approval, including election of directors and approval of certain corporate exercises or other business transactions, unless he is required to abstain from voting by law or any applicable requirements.

Nevertheless, we have appointed 4 independent non-executive Directors as a step towards good corporate governance. Our structure is such that members of our Board and key management have their own independent functions but overall decisions are made on a collective basis which will be congruent with our objectives. There are also control procedures in place to ensure business decisions and outcomes are made on a rational and independent basis and not through undue influence.

4.2.12 Security and System Disruption

We operate in an environment where our operations are exposed to risks of computer viruses, industrial espionage, theft, hacking and fraud. Security breaches on our software may lead to unexpected capital expenditure and cause a loss in revenue and reputation. Problems caused by security breaches could result in loss of or delay in revenue, loss of market share, failure to achieve market acceptance, diversion of R&D resources, harm to our reputation, customer claims, increased insurance costs and other related costs, legal suits and warranty costs.

Nevertheless, we are undertaking efforts to minimise potential security breaches by the use of appropriate security systems and firewalls, and all other necessary steps to minimise the risk of any potential security breaches. In addition, our valuable data is stored and backed-up on a regular basis to mitigate against system disruptions. To date, there has not been any material disruption or damage to our computer systems.

4.2.13 Breakout of Fire, Energy Crisis and Other Emergencies

All businesses face the risk of losses arising from emergencies such as breakout of fire and energy crisis. Our Group has taken note of such risks and has taken various steps to reduce such risks by having proper fire-fighting systems, dispersing the storing of our network equipment and carrying out periodical review on our security and maintenance. We have also taken insurance coverage such as the Electronic Equipment Insurance Policy to mitigate financial losses from such happenings where possible. In addition, we have back-up storage located in different geographical locations to minimise risks relating to the breakout of fire, energy crisis and other emergencies.

4.3 RISKS RELATING TO OUR INDUSTRY

4.3.1 Rapid Technology Changes

The semiconductor industry is characterised by rapid technological developments, evolving industry standards, changes in design methodologies, changes in customer requirements and frequent new product introductions and enhancements. Our Group's design services may become less competitive and less marketable due to the rapidly changing technology. If we do not stay up-to-date with technological advances and be sensitive to the market trends or if one or more of our Group's competitors introduce products and design services that can better address customers' needs, it may adversely affect our Group's competitiveness and therefore may affect our Group's business, operating conditions and financial results.

Our Group minimises our exposure to technological obsolescence through our ongoing R&D effort to introduce a design that is capable of high performance with a small die size and low power consumption using the latest technology which our Directors believe will adequately address the changing needs of the marketplace while keeping the cost to customers relatively low. Our Group has an experienced and skilled team of R&D personnel, which constantly endeavours to keep abreast with contemporary leading-edge technologies and carry out the necessary research to capitalise on such technologies that are suitable for our future business. We constantly encourage our key management and technical personnel to frequently attend microelectronics conference or trade shows, if necessary. However, there can be no assurance that our Group will be able to keep abreast with the changes in the technologies and that such changes would not affect our Group's competitiveness in the semiconductor industry.

4.3.2 Cyclical Nature of the Semiconductor Industry

The semiconductor industry is cyclical in nature, generally characterised by 4 recurring year cycles. Typically, these cycles had in the past recorded 2 strong years of growth, 1 year of slow growth and 1 year of flat or declining growth. The cyclical nature of the semiconductor industry poses a challenge for chip design service providers as the demand for chips is largely dependent on the performance of the global computer, communication and consumer markets.

Nonetheless, we intend to diversify our chip design products to various applications from consumer electronics to computer and communications, and to take advantage of the future growth in the industry, which would be strongly driven by the wireless and personal computer markets. This would be further augmented by the growth in the consumer electronic products as demand for new technology and multi-functional devices such as camera phones, PDAs, MP3 players and portable DVDs gains momentum.

Although we are taking the above step to mitigate the cyclical nature of the industry, we cannot assure that the measures we have taken will be adequate if there is an industry downturn and that it will not have a material adverse effect on us.

4.3.3 Inability to Achieve Economies of Scale

Although it would appear that our Group as a design house needs to only concentrate on designing chips, R&D and marketing, we also need to focus on achieving volume business, through negotiations with the foundries on favourable volume purchase. For an ASIC designer like us, since the products are "application-specific" and we are not able to enjoy wider applications as compared to the "general all-purpose" counterparts, it is essential to target large volume to achieve economies of scale for its products. In addition, ASIC designs involve a high initial design cost, including non-recurring engineering cost, which makes it profitable only if the product is able to reach high volumes with low cost. Hence, we may risk not being able to achieve economies of scale if we are not able to leverage on large volumes of designs.

To mitigate this risk, we intend to leverage on large volume production to provide us with sizeable recurring revenue. Our Group aims to capture the next version of high volume production chips and optimise the design to have higher performance, lower power consumption and small die size. We will also try to design our chips within budget or at lower costs and increase our marketing aggressiveness in order to compete with other players.

4.3.4 Lack of Control over IC Production

Unlike the IDM which is able to coordinate the various stages of IC manufacturing internally including design, manufacturing, test and packaging, and sales of IC products, our Group, as an independent IC design house does not rely on the manufacturing activities. IDMs are capable of controlling the timing and cost structure of IC production and hence, they can control a share of the marketing profits. Through growing production capability and financial clout, they can expand the size of their operations to cover increasingly greater varieties of products. Our Group seeks to mitigate this risk through continuous R&D in improving our existing design and services, maintaining good relationships with our existing foundry, creating highly skilled and qualified personnel and have efficient cost control within our Group.

4.3.5 Political, Economic and Regulatory Considerations in Malaysia

Given the nature of the industry, in which our Group operates, our operations are closely linked to the political, economic and regulatory conditions in Malaysia and other countries. Any adverse developments or uncertainties in the political, and/or international events, economic and regulatory conditions in Malaysia and other countries may adversely affect the performance of our Group. These include, among others, the risk of war, riots, expropriation, nationalisation, renegotiation or nullification of existing contracts and arrangements, global economic downturn and unfavourable changes in governmental policy such as changes in interest rates, inflation rates and methods of taxation, changes in managed foreign exchange rate and regulation or other legal, administrative, political, economic or social developments. There can be no assurance that any changes to these factors will not have an adverse effect on our Group's business and financial performance. The success of the Public Issue depends also on the prevailing market conditions which are unpredictable and volatile.

4.4 OTHER RISKS

4.4.1 Foreign Exchange Fluctuations

We sell our design services to various overseas customers. Our sales in these markets are predominantly transacted in USD. As such, our exposure to the fluctuation in foreign exchange rates may be significant and any material fluctuation in the exchange rates could have a significant impact on our profitability.

The risk of foreign exchange fluctuation is however, mitigated by the managed float mechanism adopted by Bank Negara Malaysia since July 2005 on the RM-USD conversion rate which may prevent extreme exchange rate fluctuation. At the same time, we also license our IPs from overseas and outsource certain design works to Key ASIC Inc.. These costs of sales are also denominated in USD, which provides a natural hedge, ensuring that our Group is not adversely affected by unfavourable foreign currency movements. We also maintain all our currency in RM whilst maintaining a USD foreign currency account for trade-related transactions in foreign currency.

4.4.2 Actual Results Differ from the Prospective Financial Information

We wish to highlight that our consolidated profit estimate and forecast for the FYE 2007 and FYE 2008 as set out in Section 11.7 of this Prospectus are based on assumptions made by our Directors which they believe to be reasonable at that point in time. The assumptions reflect the current judgement of our Directors on the expected conditions and course of action which are subject to uncertainties and contingencies. Many of these factors are beyond our control and some of the assumptions with respect to future business decisions and strategies are subject to changes. As such, our actual results may differ from such estimate and forecast, and the differences may be material and may affect our share price and dividend payout, if any, in the future.

You should note the bases and assumptions made with respect to the consolidated profit estimate and forecast as well as our Reporting Accountants' letter on the consolidated profit estimate and forecast as set out in Section 11.6 of this Prospectus.

4.4.3 Uncertainty in the 3-Year Business Development Plan

Our Group's future plans and prospects will depend on our ability to successfully execute the product road map; enhance or improve on our existing IPs; continue to port new IPs with our foundries, production of lower power chip and smaller die size; enhance our R&D activities; enter into strategic marketing and business development strategy; enhance our competitive strength; hire and retain skilled management as well as financial, technical, marketing and other personnel; successfully managed growth (including monitoring operations, controlling costs and maintaining effective quality and service controls); and obtain adequate financing as and when needed. Nevertheless, there can be no assurance that our Group will be able to successfully implement its business plan or that unanticipated expenses or problems or technical glitches will not occur which would result in delays in its implementation or even deviation from its original plans. In addition, the actual results may deviate from our business plan due to rapid technological changes, market changes as well as competitive environment.

4.4.4 Forward Looking Statements

This Prospectus contains forward-looking statements. All statements, other than statements of historical facts, included in this Prospectus that address activities, events or developments that we expect or anticipate will or may occur in the future are forward-looking statements. Such forward-looking statements are made based on assumptions that our management believes to be reasonable as at the date hereof. Forward-looking statements can be identified by the use of forward-looking terminology such as words "may", "will", "would", "could", "believe", "expect", "anticipate", "intend", "estimate", "aim", "plan", "forecast" or similar expressions and include all statements that are not historical facts. We expressly disclaim any obligation or undertaking to release publicly any update or revision to any forward-looking statement contained in this Prospectus to reflect any change in our expectations with regard thereto or change in events, conditions or circumstances on which such statement is based.

5. INFORMATION ON OUR GROUP

5.1 HISTORY AND BACKGROUND

5.1.1 Our Group's Historical Overview

We were incorporated in Malaysia under the Act on 22 August 2005 as a private limited company known as Pearl Discovery Sdn Bhd. On 3 October 2005, we changed our name to Key ASIC Sdn Bhd. Subsequently, we were converted into a public limited company on 13 June 2007 and assumed our present name. On 14 April 2006, we were awarded the MSC status by MDeC and are currently enjoying full income tax exemption under the pioneer status for a period of 5 years and renewable for another 5 years.

Our Company is principally engaged in fabless high-end turnkey ASIC/SoC design services and development of IPs whilst our subsidiary is principally engaged in the business of providing manufacturing management services to fabless design companies, provide design-for-manufacturing and design-for-test consultation and the sale of wafer and SoC products. The manufacturing process of the chips is outsourced to foundries and manufacturing partners. We are able to provide design-to-manufacture services through close partnership with foundries and other test and packaging houses.

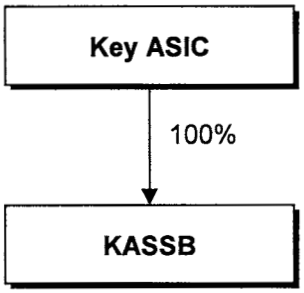
We commenced operations on 22 August 2005 as a wholly-owned subsidiary of KAL. We started our design activity by designing IPs and also application specific SoC platforms. These IPs are essential building blocks for SoC chips for consumer electronic and communication applications. The consumer electronics applications include MP3, PMP, DVB, DVD, digital home gateway and image processing chips. The IPs for the communication applications includes VoIP, xDSL, Wi-Fi and WiMAX.

In the beginning of 2006, we developed and ported our first set of analogue IPs on 0.18µ process technology of Silterra. Subsequently, the second set of IPs that we ported on 0.18µ and 0.13µ process technology of Silterra were ARM 926, ARM 946 CPU cores and interface IPs. Currently, we have more than 50 peripheral IP blocks developed and ported on Silterra's 0.18µ, 0.16µ and 0.13µ technology and some of the IPs were also developed and ported on other foundries such as TSMC.

Our core competence is the capability of our design team to design SoC and ASIC from system specification and architectural level to GDS II. The key differentiator of our Company is our expertise in designing high performance, low power consumption and smaller size chips. We are also capable of designing low power chips for mobile devices. Currently, we have two operations in Malaysia and they are located in Petaling Jaya and Cyberjaya.

As part of our 3-year business plan, we are focusing on developing our IPs to target consumer electronics and communication due to the growth of this market segment from the use of devices such as MP3, mobile phones, PDA and portable players. With continuous push for performance, low power consumption and smaller die size for most hand held devices, we plan to port our IP and platforms to smaller IC size to 0.09µ and 0.065µ in 2008 and 2009 respectively. We plan to expand our application platforms and plan to develop some IPs for new application needs.

Our Group structure can be depicted as follows:



Further details on our Group's business and industry are set out in Section 5.4 of this Prospectus.

5.1.2 Share Capital

The present authorised share capital of our Company is RM100,000,000 comprising 1,000,000,000 Key ASIC Shares. The issued and paid-up share capital of our Company is RM60,300,000 comprising 603,000,000 Key ASIC Shares. As at the date of this Prospectus, neither our Company nor our subsidiary has any outstanding warrants, options, convertible securities and uncalled capital.

Details of the changes in the issued and paid-up share capital of our Company since its incorporation are as follows:

Date of allotment	No. of shares	Type of shares	Par value RM	Consideration	Total issued and paid up share capital RM
22.08.2005	2	Ordinary shares	1.00	Subscriber shares	2
05.04.2006	32,299,998	Ordinary shares	1.00	Capitalisation of amount owing to holding company	32,300,000
14.07.2006	19,000,000	Preference shares	1.00	Issuance of ICPS	51,300,000
04.10.2007	19,000,000	Ordinary shares	1.00	Conversion of ICPS	51,300,000
19.11.2007	9,000,000	Ordinary shares	1.00	Rights Issue	60,300,000
21.11.2007	603,300,000	Ordinary shares	0.10	Share Split	60,300,000

Our issued and paid-up share capital would subsequently increase to RM80,500,000 comprising 805,000,000 Shares following our Public Issue.

5.2 LISTING SCHEME

5.2.1 Restructuring

In conjunction with, and as an integral part of our Listing on the MESDAQ Market of Bursa Securities, we undertook a restructuring exercise involving the following:

(i) Conversion of ICPS

Our ICPS holders, namely AQSB and CTVSB have converted their ICPS amounting to 19,000,000 into ordinary shares based on the conversion of 1 new ordinary share of RM1.00 each in Key ASIC for every 1 existing ICPS held in Key ASIC.

The conversion was completed on 4 October 2007, and resulted in our share capital being enlarged to RM51,300,000 comprising 51,300,000 ordinary shares of RM1.00 each in Key ASIC.

The new ordinary shares of RM1.00 each in Key ASIC, with effect from the conversion date, rank equally in all respects with our existing issued and paid-up ordinary shares. This includes voting rights and entitlements to all rights, dividends and other distributions that we may subsequently declare after the conversion.

(ii) Rights Issue

We have implemented a renounceable rights issue of 9,000,000 new ordinary shares of RM1.00 each in Key ASIC at an issue price of RM1.00 per share on the basis of about 175 new ordinary shares of RM1.00 each in Key ASIC for every 1,000 existing ordinary shares of RM1.00 held in Key ASIC.

The Rights Issue was completed on 19 November 2007 and resulted in our share capital being enlarged to RM60,300,000 comprising 60,300,000 ordinary share of RM1.00 in Key ASIC.

(iii) Share Split

Upon completion of the Rights Issue, we implemented a share split on the basis of 1 existing ordinary share of RM1.00 in Key ASIC held into 10 Key ASIC Shares.

The Share Split was completed on 21 November 2007 and resulted in our number of shares increasing to 603,000,000 Key ASIC Shares.

5.2.2 Public Issue

In conjunction with the flotation of our Company on the MESDAQ Market of Bursa Securities, our Company will make available 202,000,000 Issue Shares as follows:

(a) 10,000,000 of the Issue Shares available for application by the Malaysian public;

(b) 16,500,000 of the Issue Shares available for application by our eligible Directors, employees and business associates; and

(c) 175,500,000 of the Issue Shares available for private placement to institutional investors and selected investors.

5.2.3 Listing

Thereafter, we will seek an admission to the Official List of the MESDAQ Market of Bursa Securities for the listing of and quotation for our entire enlarged issued and paid-up share capital of RM80,500,000 comprising 805,000,000 Key ASIC Shares.

5.3 SUBSIDIARY

As at the date of this Prospectus, we have a subsidiary, namely KASSB, the details of which are as follows:

Name	Date and place of incorporation	Issued and paid-up capital RM	Effective interest %	Principal activities
KASSB	07.06.2007; Malaysia	2	100.00	Provision of manufacturing management services to fabless design companies, design-for-manufacturing and design-for-test consultation, and sale of wafer and SoC products

As at the date of this Prospectus, we do not have any associated company.

5.3.1 KASSB

(i) History and Business

KASSB was incorporated in Malaysia under the Act on 7 June 2007 as a private limited company under its present name. KASSB is principally involved in the provision of manufacturing management services to fabless design companies, design-for-manufacturing and design-for-test consultation and sale of wafer and SoC products. KASSB commenced business operations since its incorporation.

(ii) Share Capital

The present authorised share capital of KASSB is RM100,000 comprising 100,000 ordinary share of RM1.00 each in KASSB. The issued and paid-up share capital is RM2 comprising 2 ordinary share of RM1.00 each in KASSB.

Changes in the issued and paid-up share capital of KASSB since its incorporation are as follows:

Date of allotment	No. of ordinary shares	Par value RM	Consideration	Total issued and paid-up share capital RM
07.06.2007	2	1.00	Subscriber shares	2

(iii) Substantial Shareholder

KASSB is our wholly-owned subsidiary.

(iv) Subsidiary and Associated Company

As at the date of this Prospectus, KASSB does not have any subsidiary or associated company.

5.4 BUSINESS OVERVIEW

Our Company is principally engaged in fabless high-end turnkey ASIC/SoC design services and development of IPs whilst our subsidiary is principally engaged in the business of providing manufacturing management services to fabless design company, providing design-for-manufacturing and design-for-test consultation, and the sale of wafer and SoC products.

5.4.1 Principal Products and Services

Our Group's design services include providing customers with one-stop design-to-manufacture integration services via our in-house capabilities and we have formed strategic partnerships with semiconductor foundries and other test and packaging houses. Through KASSB, we manage the entire design value chain starting from customers providing us with top-level technical specification and us providing architectural design down to outsourcing the fabrication process to a foundry. In this case, we act as a contractor to the customers. We add value to the intermediate stages of the development by organising foundry, integration and assembly, final test and shipment services in order to deliver volume production of final products, tested and packaged. Apart from the ASIC design, we also provide design-to-manufacturing and logistic services to the customers. Our complete SoC design flow covers system, front-end and back-end design, depending on the customers' desired involvement in the SoC design. This can be seen as a one-stop turnkey solution to the customers.

Customers' engagement can begin at three different levels, ranging from high-level specification to GDS II as follows:

(a) Design from specification

Customers provide us with detailed specification of the ASIC and our design engineers will design from specifications at RTL codes, go through RTL simulations, perform synthesis and gate level simulations. Upon successful completion of the gate level simulation, we will perform the physical implementation, place and route, DRC/ERC extractions, and post layout timing analysis before producing a GDS II file. From here, we can also deliver customers with tested and packaged chips or wafers through our collaboration with foundry and testing houses if customers desire.

(b) From Netlist

Additionally, customers can provide us with a thoroughly verified netlist and we will provide the place and route services and extraction. From here, we can also deliver customers with tested and packaged chips or wafers through our collaboration with foundry and testing houses if customers desire.

(c) From GDS II

Alternatively, customers can complete the entire design in-house and provide us with a GDS II file. From here, we can also deliver customers with tested and packaged chips or wafers through our collaboration with foundry and testing houses if customers desire.

Through our KeyIP services, we also offer customers access to IP from our pool of silicon-proven mixed-signal and digital IPs, including interface, IP blocks, CPU and DSP that is targeted for designs of PMP, MP3 players, cell phones, Wi-Fi, WiMAX, set top boxes, digital home media servers, multimedia, networking, VoIP and telephone products. We design, develop and license our IPs to customers worldwide. We have developed a complete set of IPs, namely KeyWare targeted at the consumer electronics and communication segment. We also provide IP porting service and full custom IP design service to the exact specification from customers. Currently, we have more than 50 peripheral IP blocks developed and ported. Our IP portfolio covers a variety of baseline IPs and application IPs. We are a full range ASIC design service provider. Our IP category library and applications are listed below:

5. INFORMATION ON OUR GROUP *(CONT'D)*

Audio/Video IPs	VOIP	WiFi	MP3	DVD recorder	Set-Top Box	Image Processor	Multimedia server	PMP
DAC	√	√	√	√	√	√	√	√
ADC	√	√	√	√	√	√	√	√
Audio Codec	√		√	√	√		√	√
Voice Codec	√		√	√	√		√	
DVI				√			√	√
Power Management								
LDO Voltage regulator	√	√	√	√		√	√	√
DC/DC converter	√		√	√		√	√	√
Power on Reset	√			√			√	√
BandGap	√	√	√	√			√	√
Connectivity								
802.11a/b/g/n AFE	√	√						√
PCIx/ PCIe		√					√	
SATA				√	√	√	√	√
Ethernet 10/100	√	√			√	√	√	
FireWire 1394				√		√	√	
USB2.0	√	√	√	√	√	√	√	√
DDR					√		√	
PATA				√		√	√	
I/O								
Programmable CUP I/O	√	√	√	√		√		√
HSTL/ SSTL					√		√	
LVDS		√		√	√	√	√	√
CE-ATA/MMC						√		
Universal Cardbus					√			
MISC								
RTC	√		√	√	√	√	√	√
PLL	√	√	√	√	√	√	√	√
High Speed datapath KEYWARE	√	√	√	√	√	√	√	√
ROM	√	√	√	√	√	√	√	√
SRAM	√	√	√	√	√	√	√	√
RF	√	√	√	√	√	√	√	√
High Density standard cells	√	√	√	√	√	√	√	√
DLL					√		√	
CPU								
ARM926EJS	√	√	√	√	√	√	√	√
ARM946ES	√	√	√	√	√	√	√	√
High Speed ARM926EJS	√	√	√	√	√	√	√	√
Low power ARM926EJS	√	√	√	√		√		√

Figure 1 : IP Category Library and Application

There are 4 components of revenue received for our services, which comprises non-recurring engineering ("NRE") charges, IP licensing fee, royalty fee and sales of chips.

- NRE charges are one time charges for the engineering effort in designing the chips or IP. Customers would have to pay a higher non-recurring engineering charges if there is customisation or if they require certain specification to the design of the chips;
- IP licensing fee is a licensing fee charged for the usage of the IPs in customer designs;
- Royalty fee is a recurring income paid by customers to our Group for every chip manufactured using the IP licensed from us; and
- Sales of chips are the sales of completed chips in the form of packaged chips or wafer.

The diversified revenue model helps our Group to ensure business sustainability and reduces dependency on any single source of income.

One of the key distinctive features of our Group's services in comparison with the services provided by our competitors, that would attract repeat orders from customers is that our strategic partnership with Silterra allows us to have preferential access to Silterra's foundry capacity, providing us a short turnaround time and on-time delivery. Additionally, given the lower engineering and premise rental cost in Malaysia, we can generally offer a better price to our customers around the world as compared to our competitors from Taiwan, Singapore and USA.

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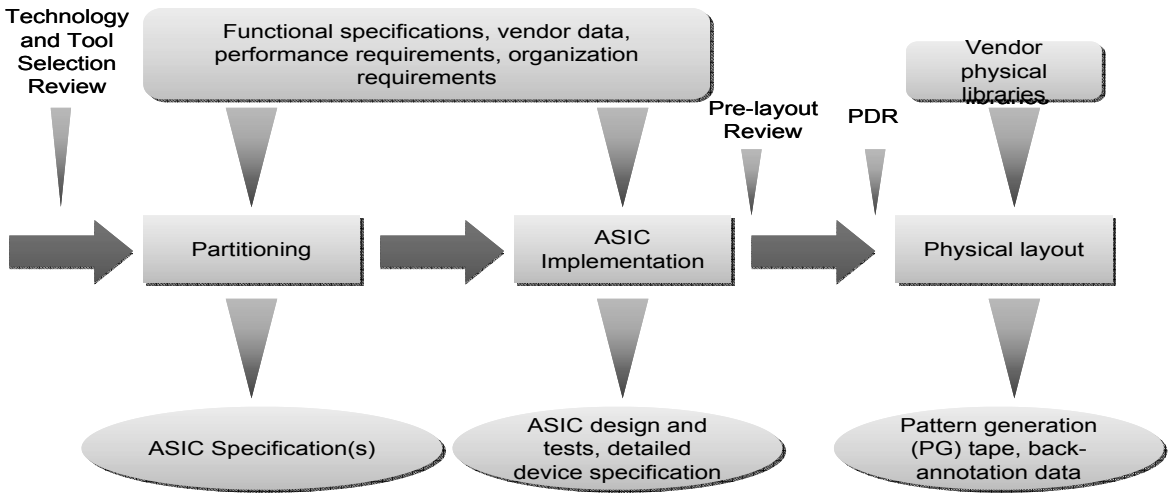
5.4.2 Design and Production Flow

Design Flow



Production Flow

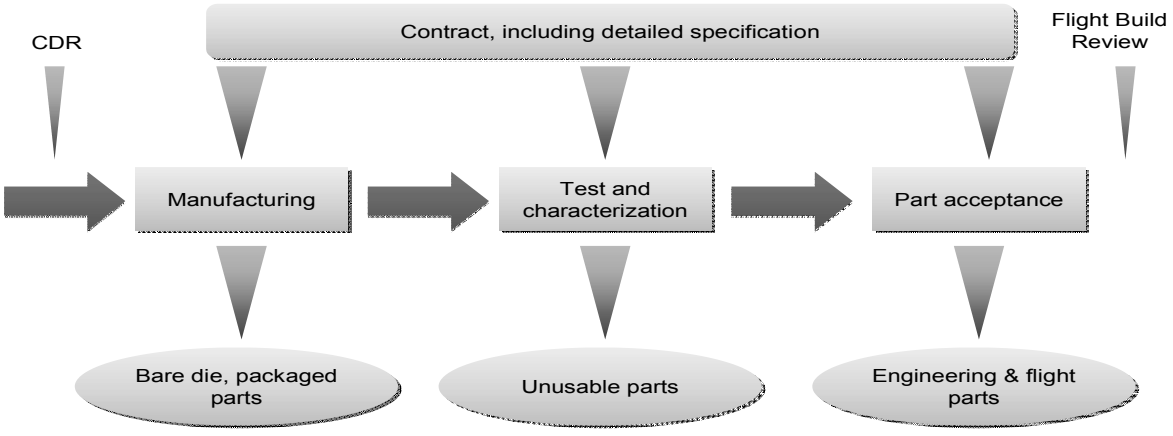


Figure 2: ASIC Design Flow

Figure 2 above illustrates the entire design and production flow for ASIC and SoC of Key ASIC. The ASIC design flow is the major engineering development for our Group and will be the design environment platform for all products in our future development. The flow is illustrated in a simple and rough chronological, single-threaded sequence.

5. INFORMATION ON OUR GROUP *(CONT'D)*

The following is the description of the major process of the above ASIC flow:

Partitioning is the process to carve out the correct part of the system for implementation as an ASIC. The system architects and ASIC designers will perform general partitioning from the time system level specifications are laid out. Test and performance requirements, global device specifications such as testability specification and functional specification must be taken into account during the partitioning process. In this process, the system architects will do the system level performance verification to verify the logic partitioning.

The **ASIC implementation** delivers a complete ASIC design and associates the design with complete verification test programs. For ASIC design, the primary emphasis is on the optimum use of resources to satisfy specific performance, reliability and cost requirements. The ASIC implementation has to come along with its verification and testability analysis. The verification including simulation and test vector generation are the most important events of an ASIC implementation. The ASIC implementation methodology focuses on first-pass successful silicon. The first-pass successful silicon would mean an ASIC device built from the first preliminary design review ("PDR") and critical design review will work correctly in its system and require no redesigning.

Physical layout is ASIC design at the final level. The ultimate result of this design work are fabrication masks used to build ASIC parts. Physical layout is done through place and route using foundry provided physical libraries after the PDR sign-off. After completing the layout, the designers review the back-annotated resistance and capacitance values arising from the inter-connects in the physical layout. These numbers reflect reasonable estimates of the final design's worst case and best case performance. This review consists of post-layout simulation and path analysis to make sure no significant changes in functional and performance have occurred because of layout.

The **manufacturing** process is to produce ASIC dice assembled into packages. The manufacturing process consists of 3 phases which comprise wafer fabrication, wafer probing using automated test equipment and prober, and assembly process by separating dice from wafer and assemble into package unit. We do not have wafer fabrication facilities, hence we outsource our fabrication processes to Silterra, our foundry partner. The wafer fabrication process requires approximately 6 to 10 weeks for completion.

Testing and characterisation ensures that the manufactured parts meet the goals of the ASIC design. The ASIC chips have to meet the testing and characterisation outlined in the contract. The characterisation focuses on electrical, performance and power characteristic of the chips. Currently, the physical test and packaging of the chips are also outsourced to our test and packaging partner, ASAT Holdings Limited.

Part acceptance applies quality and reliability criterion to parts delivered for prototyping and engineering samples. This process will screen out devices that show potentially serious problems. Upon completion of this process, the final end product will be delivered to the customers.

5.4.3 Principal Market

Figure 3: Market segment

Figure 3 above describes the market segments in our industry. Semiconductor or IC is a global business in nature. Companies in the semiconductor market compete based on technology and selling capability. According to the Directors of Key ASIC, most of the fabless design companies in the world today design mainly ASSP products. However, there are only limited fabless design companies, including our Group, that have its own technologies and capabilities to design a process technology specifically into a foundy process directly using their own IP, PDK and design flow. Usually, our customers are the fabless design houses, IDM, system ASIC companies and COT companies. We have made our mark with some leading customers in USA, Europe, Taiwan and Malaysia. Our services are usually targeted at consumer electronic and communication market such as PMP, MP3, digital audio player, set top box, digital TV, digital media broadcast, digital imaging, mobile phones and wireless network. Moving forward, we will focus on capturing turnkey design businesses in China, Japan and Korea.

5.4.4 Technology Used

Our Group's primary technology is the KeyPlatform for ASIC and SoC design-to-manufacture that aims to reduce customer design time and allow first time silicon success.

KeyPlatform is a technology that comprises our design methodology and software used, coupled with our own IPs developed. The platform provides a high performance ARM-based CPU platform with CPU core and memory blocks, for integration of domain specific IP blocks to design a specific SoC quickly. A wide variety of mixed analogue digital IP blocks, memory blocks of different sizes and speed, high quality audio and voice codec, and peripheral interfaces are available for quick integration of a chip. The platform also consists of a wide selection of silicon proven interfaces such as USB2.0, IEEE 1394, ETHERNET, PCIe, and many others.

The system and circuit design steps are aided by the use of EDA tools. These EDA tools are software tools used by our designers for the development of chips and systems. The EDA tools allow the creation and simulation of the chip functionalities and performance. The usage period of the EDA tools are governed by their respective licensing terms.

5.4.5 Mode of Marketing

Marketing of our services comprises design introduction to potential customers, discussions with customers on the application of the chips and obtaining system designs contract. We would normally require an upfront commitment from our customers before we commence any design work. As part of our sales strategy, we would also design for our customers based on a memorandum of understanding signed in the effort to attract repeat orders from customers by offering lower wafer cost. We are able to offer lower wafer cost as compared to our competitors due to our strategic partnership with Silterra allowing us to have preferential access to Silterra's foundry capacity as well as the lower engineering and premise rental cost in Malaysia. For those customers with large volume demand, we would design without collecting a design fee upfront as the fees are usually incorporated into the wafer price.

Our direct sales team is headed by Mr. Chan Woo Nam, our designated Vice-President of Strategic Accounts pursuant to a Management Agreement dated 1 January 2006 to which we have appointed Key ASIC Inc. to sell and market our services in all countries, other than Malaysia, subject to us also having the rights to continue marketing our own services. Key ASIC Inc. has appointed Mr. Chan Woo Nam as a representative to act as liaison with our Group and shall maintain a dedicated team of sales, marketing and technical support personnel in the region to visit prospective customers and provide timely feedback to us on the technical requirements of customers in relation to the product and sales requirements and engage customers to secure business with our Group. Key ASIC Inc. will facilitate the conclusion of definitive agreements to be signed by us directly with customers.

The strength of our sales team is also coupled with the experiences, business relationship and network of some of our Directors, namely Benny T. Hu and Eg Kah Yee, to which both are very instrumental and capable in assisting our Group in bringing in businesses.

Our marketing strategy is not just to target our services to fabless design houses, but also the IDM, system ASIC companies and COT companies. We intend to focus our marketing effort towards the consumer electronics and communication industry with the intention of customising and developing of ASIC and SoC for their applications. We will focus on high end turnkey market where most design houses do not have the capability in designing. Designs such as audio/video or multimedia communication and networking are areas of our focus.

We market our services through various platforms including technology forums, seminars, website, electronic mails and participation in conferences and trade shows. In addition, we also organise joint marketing programmes with foundries, IP partners, design service partners and IC component distributors.

Our sales strategy is to have high volume production chips to achieve economies of scale and to provide our Group with sizeable recurring revenues. We will capture the next version of high volume production chips and optimise their designs to have higher performance, lower power consumption and small die size, hence giving the chips a better price/performance ratio. We will maintain a strong team of system designers with broad chip design knowledge to promote and support our services.

5.4.6 Quality Control Procedures

In order to provide high quality IPs and ASIC design services, our Group has established distinct quality policies to achieve its goals through continuous improvements as follows:

(i) To ensure precise efficiency by strictly obeying the standard operating procedures;

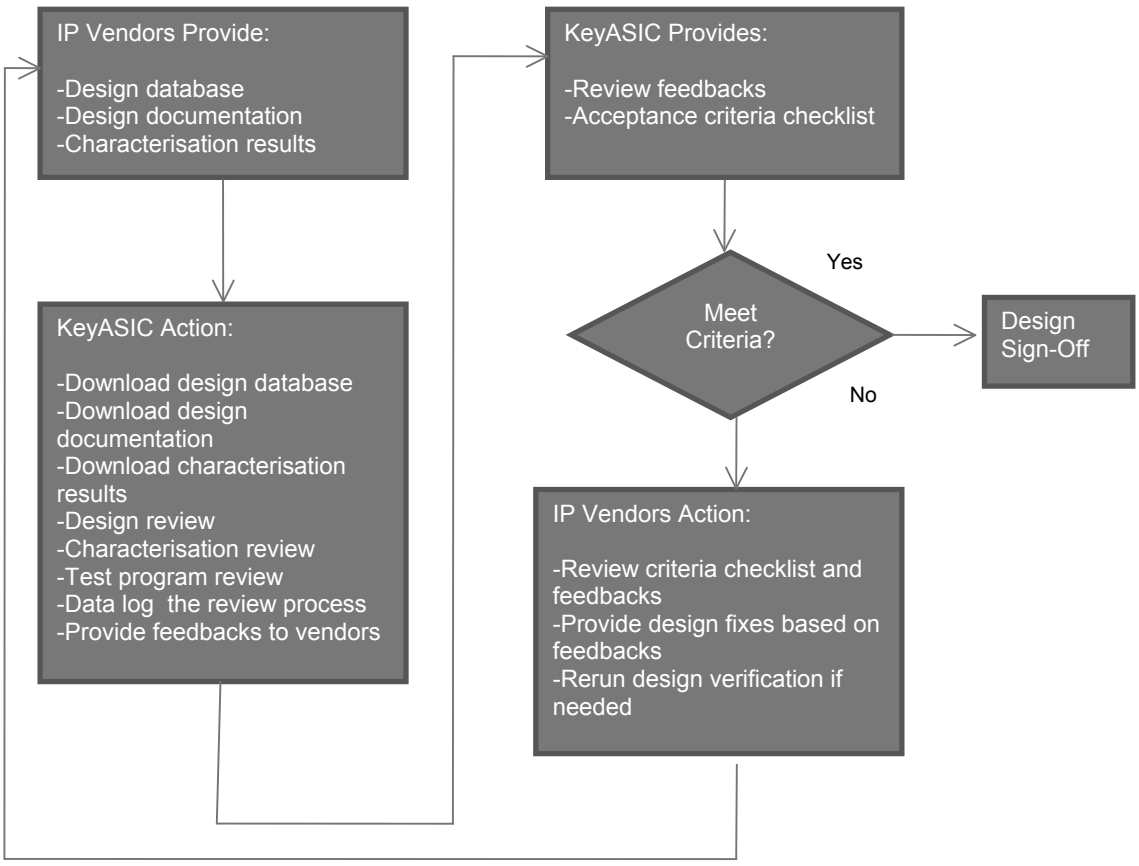
(ii) To constantly improve total quality by implementing quality management procedures;

(iii) To stay ahead of customers' needs by constantly scanning the global market for new development; and

(iv) To maintain technological lead by providing an aggressive commitment to R&D.

We practice the following quality control and management procedures as described below:

(a) IP Sign-Off Process



5. INFORMATION ON OUR GROUP *(CONT'D)*

The above diagram illustrates our IP sign-off procedures. The quality control begins at the initial checkpoint when IP vendors provide the design database, design documentation and characterisation results to our Group through our secure File Transfer Protocol ("FTP") or Virtual Private Network ("VPN"). Subsequently, our design engineers will download the design database and documentation, and conduct a design review based on a standard review design checklist. Once our design engineers are satisfied that the design meets all the criteria of the checklist, they will accept the design checklist and provide all their feedback to the IP vendors if there is any design error. Thereafter, the IP vendors would have to review the criteria of the checklist and the feedback, and provide design fixes based on the feedback. The design review will begin at the initial checkpoint again once the design error is fixed. However, if there is no design issue found, the design is considered as complete and our design engineer will sign-off the design.

(b) Design Release Process